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A CMOS SUBSCRIBER LINE AUDIO PROCESSING CIRCUIT INCLUDING ADAPTIVE BALANCE

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ABSTRACT

The increasingly sophisticated requirements of Telecommunications Operating Companies are driving component manufacturers towards providing additional features on the device commonly known as a "combo" or "cofidec". These components have been primarily analogue signal processors but the increasing availability of processing power on modern CMOS technology has allowed alternative architectures to be explored. A predominantly digital architecture allows the addition of extra features while increasing consistency and manufacturability of the product.
Analogue content of such a part is reduced to low component count analogue to digital (A-D) and digital to analogue (D-A) conversion using oversampled low word length techniques. These analogue interfaces must have a dynamic range in excess of 90dB which has to be achieved in the presence of large amounts of digital switching noise making them the most challenging part of the design.

INTRODUCTION

The design of the Plessey Subscriber Line Audio processor Circuit (PSLAC) to provide a component with the features and flexibility required in a modern digital system is described. Features include self adaptive trans-hybrid balance, fully programmable frequency response filters in transmit and receive paths, dynamic PCM time and clock slot selection and selectable A, Mu or linear PCM coding. The design made extensive use of the PLESSEY MEGACELL (reg.TM.) design suite to accelerate the process and to ensure that the silicon was correct and properly toleranced for first time operation. A block diagram of the PSLAC is shown in figure 1. The transmit path consists of highly oversampled A-D conversion followed by decimation to 16kHz. At this point the main digital signal processor takes over providing programmable gain and filtering as well as fixed filtering to CCITT specification. The signal is finally compressed to either 'A' or 'Mu' laws before being output on one of two PCM ports according to programming. The receive path provides these functions in reverse order using the same processor as the transmit path. This processor in addition realises a filter between receive and transmit paths to allow cancelling of the local echo giving improved trans-hybrid loss. This filter can be used in one of two modes, fixed or adaptive.. In the former, the coefficients are set to provide maximum trans-hybrid loss to a specified load impedance. In the second, more powerful mode, the coefficients can self adapt to improve on the performance obtained with unknown or changing load impedance. The device was required to exceed CCITT specifications G712 and G714 with up to 12dB of additional transmit gain and receive loss. The CMOS process chosen limited operation to a single 5 volt power supply. This made the dynamic range targets more difficult to meet as well as complicating the analogue interfaces to ground centred signals.

ANALOGUE INTERFACE - TRANSMIT PATH

The PSLAC is intended for operation together with the Plessey Subscriber Line Interface Circuit (PSLIC) to provide the remainder of the line interface BORSCHT functions. These circuits generally have analogue interfaces referenced about ground to which the PSLAC must interface using minimal external components. Direct interface to the PSLIC transmit output is possible. An input level shift and attenuation circuit is combined with a 1st order lowpass filter. This is followed with a second order passive lowpass filter to complete the anti-aliasing specification, figure 2. In this way only a single polysilicon resistor is biassed outside of the single +5 volt PSLAC power supply voltage range. The input signal is now referenced about an internally generated 2.5 volt reference and is buffered prior to driving the A-D converter.
A-D conversion is performed with an oversampled delta sigma modulator. Input samples to this modulator are indirectly quantised by a coarse quantiser (a low bit A-D). These quantised samples are then subtracted from later input samples and the difference is integrated. The effect of this feedback and integration is to reduce the average quantising error to zero. The basic principle of this technique, [1,2] is to translate the quantisation noise from in-band to high frequencies which is subsequently removed with digital filtering. This approach allows analogue circuit precision and complexity to be reduced at the expense of increased sample rate and increased digital processing. A single bit coder, figure 2, was chosen to minimise complexity, this reduces the A-D requirement to a simple comparator and the D-A to a pair of reference voltages.
Input voltage is represented by the long term average of the coder output samples. At DC voltages close to sub-multiples of the coder output levels 'patterning' can occur resulting in generation of large in-band components which cannot be filtered

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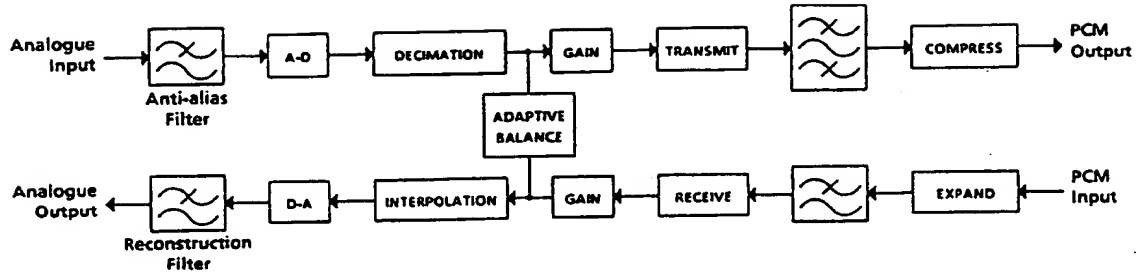

Fig. 1 PSLAC Block Diagram

from the vanted signal. A second order coder requiring two integrators was therefore necessary to spread out these components and reduce their level belov that of the noise floor.
Switched capacitor designs were chosen to realise the integrators due to their vell defined time-constants and small size. Conventional stray insensitive designs were used together with a correlated double sampling (CDS) technique, [3] to reduce the effect of amplifier offset and lov frequency (flicker) noise. Clock speed was chosen to achieve a sufficient theoretical dynamic range together with a practical settling time requirement from the switched capacitor integrators. Dynamic range of a perfect 2nd order single bit coder has the following theoretical dependance on clock frequency.

Clock Frequency	Dynamic Range (0 to 3.4kHz)
512kHz	83dB
1024	98
2048	113
4096	128

The design target of CCITT G714 plus 12dB requires a coder dynamic range in excess of 90dB. To allow sufficient margin for degradation due to component imperfections a clock speed of 2.048MHz vas chosen. This required amplifiers with a settling time to 0.1% accuracy of less than 220nS, (alloving for generation of non-overlapping clocks). These amplifiers must also have good wideband noise performance and operate over a large output voltage range. Amplifier design is based on the current gain principle and is load capacitance compensated. Large area transistors are used to obtain the required noise performance.

ANALOGUE INTERFACE - RECEIVE PATH

D-A conversion is realised using the same principle as the transmit path, figure 3. The same target of CCITT G714 plus 12dB indicates a dynamic range requirement of again around 90dB. Minimal circuit complexity dictates a lov bit D-A converter. A further requirement vas to limit out of band noise to reasonable levels using only a simple analogue reconstruction filter. A four bit D-A converter proved to be optimum. This converter is realised using 15 matched current sources vhose current is switched between one of two matched output resistors. In this vay a voltage output is obtained that is 11 bit accurate.
A digital second order delta sigma demodulator is employed to generate 2MHz samples of 4 bit data from 128kHz 18 bit data samples. The digital delta-sigma demodulator employs two 20 bit digital integrators and is operated with two bit at a time arithmetic running at 20MHz, (2MHz integration speed).
The D-A converter is followed by an analogue level shift and first order reconstruction filter stage vhose output voltage is referenced about an internally generated 2.5 volt reference. An external component is therefore required to AC couple this analogue interface to the PSLIC receive input.

ADDITIONAL ANALOGUE CIRCUITS

A stable voltage reference vas required to provide an internal ground reference, level shift referencing and D-A references for both of the

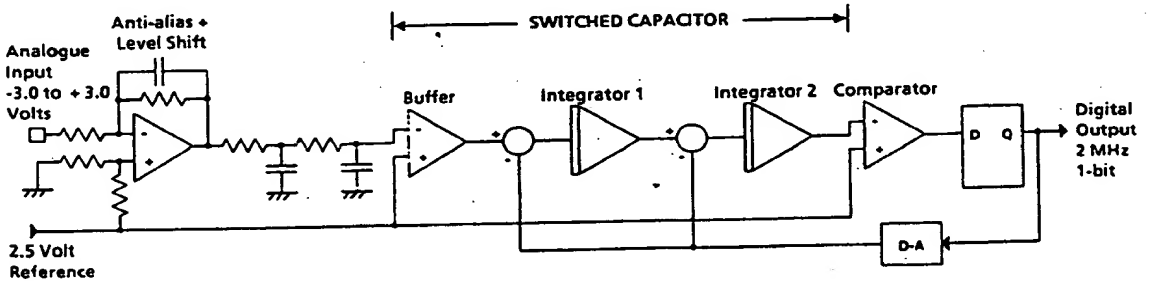

Fig. 2 Transmit Path Analogue Interface

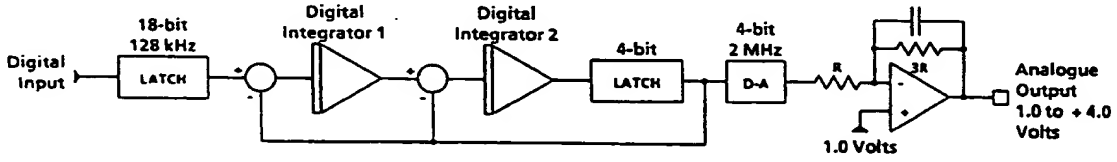

Fig. 3 Recieve Path Analogue Interface

analogue interface circuits. A bandgap design was necessary to achieve the required voltage and temperature stability. This used ratioed substrate bipolar transistors to generate a reference of nominally 1.28 volts. External decoupling of this reference is necessary to reduce its in-band noise and prevent it from limiting dynamic range of either analogue interface. This reference is followed by a trimmable DC gain stage to generate 2.5 volts. Trimming of this reference is necessary at circuit probe test to meet the specification for absolute gain through each transmission path. The trimmable components are realised as polysilicon links which can be selectively fused by applying sufficient voltage across them.

A phase locked loop (PLL) circuit is required to generate the required high speed clocks for the digital processing from a standard 2.048MHz clock. A voltage controlled oscillator (VCO) based on a standard ring oscillator is used together with a phase detector, charge pump and simple RC filter to generate a 20.48MHz master clock from which all clock generation is made.

DIGITAL ARCHITECTURE

The PSLAC is partitioned into two processors which handle the majority of the digital filtering functions. The first consists of a micro-sequenced serial-parallel processor running at a 20MHz clock rate. This processor provides the fixed coefficient high speed decimation and interpolation to a data rate of 16kHz. These filters are based on dual branch IIR filter structures, [4] with inherent low noise, good stability and low group delay. The in-band phase and amplitude distortion of these filters is very low, this is important for best performance of the trans-hybrid balance filter. An instruction rate of 2uS is used with each instruction performing up to one 18 by 12 bit multiply and four 18 bit additions. These filter structures require only two different coefficients simplifying the multiplier to require only five serial full adders.

The second processor is micro-sequenced, fully parallel, has a 10MHz clock rate and performs all of the programmable filter functions including adaptive balance in addition to the fixed CCITT bandpass filtering. This processor, optimised for this function, has an 18 bit ALU, three adders with registers and an 18 bit (data) by 12 bit (coefficient) two's-complement Baugh-Wooley multiplier and operates at a 1uS instruction rate. Coefficients for gain and frequency response adjust filters for both signal paths and those for the trans-hybrid balance filter are programmable via an external serial control port and are stored in RAM within this processor.

In addition a self adaptive mode of operation for the balance filter may be selected which attempts to minimise the level of transmitted echo with varying local line and telephone parameters. This echo would otherwise impair transmission or at worst cause instability. The adaption algorithm is based on the Least Mean Square (LMS) approach and has been designed to be as robust as possible. The number of multiplications required are reduced to only one per tap per cycle by using the following clipped LMS algorithm.

$$CAj_{n+1} = CAj_n + (\mathrm{Sgn}\ X_j).e_n \qquad (1)$$

where CAj_n = Adaptive Coefficient of jth tap at t=n

$\mathrm{Sgn}\ X_j$ = sign of current data sample

e_n = B.(adaptive error), B = constant

This reduces the amount of coefficient change as the error becomes smaller. Adaption vill operate

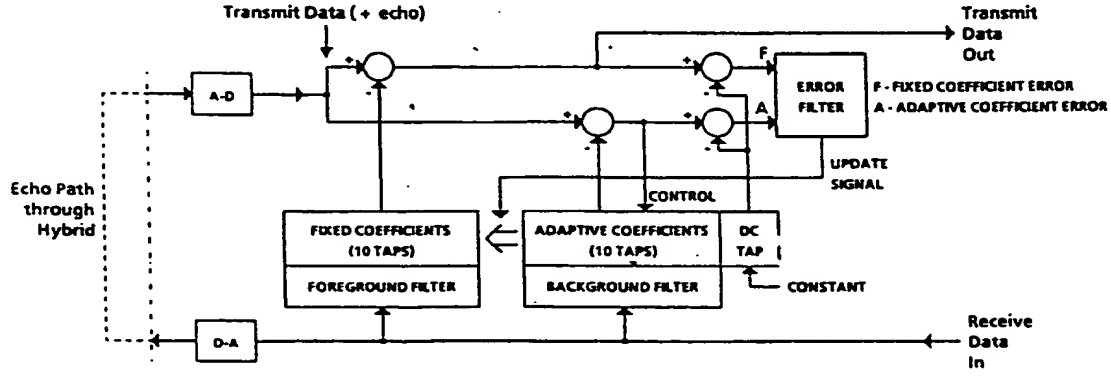

Fig. 4 Adaptive Balance Filter Block Diagram

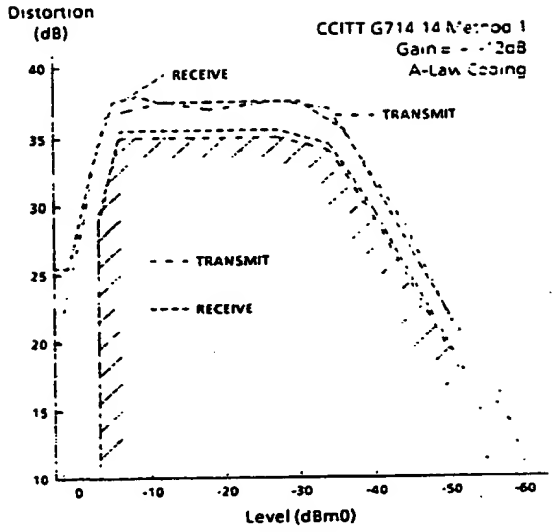

Fig 5 Typical Signal to Distortion Measurement

over a vide range of signal conditions including a limited amount of doubletalk and does not suffer from coefficient instability when very large signals occur, or during severe doubletalk. This is achieved by implementing the balance filter using two 10 tap FIR filters, figure 4. A fixed foreground filter is used for echo cancellation, with the coefficients for the fixed filter being derived from an adaptive filter operating in parallel with it. Whenever the long term average of the adaptive error is considerably less than the fixed error the error filter produces an update signal to transfer the adaptive coefficients to the fixed filter. In this arrangement the adaptive filter is alloved to diverge during periods of doubletalk with the error filter inhibiting update of foreground filter coefficients. A DC tap is included to allov adaption in the presence of large DC offsets in the transmit path.
Additional dedicated hardvare is used to implement a triangularly veighted filter to perform initial stages of decimation from 2MHz to 256kHz and to implement a PCM compander for compression and expansion to provide external interfaces to 'A', or 'Mu' laws, CCITT G711.

PERFORMANCE

The design vas realised on a standard 2um CMOS process with double layer metalisation using a silicon area of 43 mm^2. The device is assembled in a 28 pin DIL package and requires only a single external component. Measured performance exceeded the design target, figures 5 and 6 show typical transmit and receive signal to distortion and gain linearity performance measured with maximum (12dB) gain and loss. The use of a single bit coder results in an inherently linear and distortion free transmit path. Very repeatable performance has been obtained due to the use of digital signal processing techniques with only a few non-critical analogue components.

Performance of the adaptive balance filter is difficult to quantify as this is very dependant on individual line and telephone impedances. In general an Echo Return Loss Enhancement (ERLE) in excess of 30dB is achievable across the pass-band. Adaption time is very dependant on local and far end speech content although typically might be a few hundred milliseconds.

CONCLUSIONS

The design of a Subscriber Line Audio Processing Circuit including self adaptive trans-hybrid balance has been described. Its transmission performance has been shovn to exceed CCITT specifications with up to 12dB of transmit gain and receive loss. This has been achieved using a single 5 volt power supply while maintaining simple analogue interfaces to a Subscriber Line Interface Circuit. This circuit will enable the design of programmable and flexible line cards giving superior transmission performance over those realised with more conventional components.

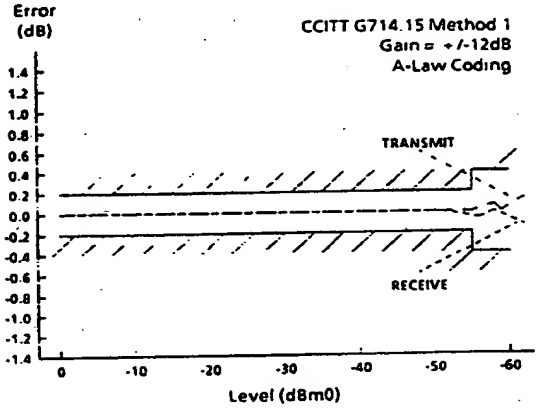

Fig 6 Typical Gain Linearity Measurement

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